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lec 3
ch 7

Sheet #4

1- We need MFC step when reading from or writing to the main memory →

to syncheronize the operation of the processor and the main memory.

2. Given Figure 7.6 Add (R3), R1

Step	Action	Problem 2: Clock cycle	Problem 3	Problem 7	
1.	PCout, MARin, Read, Select4, Add, Zin	1	1		2ns
2.	Zout, PCin, Yin, WMFC	1	2		16ns
3.	MDRout, IRin	1	1		2ns
4.	R3out, MARin, Read	1	1		2ns
5.	R1out, Yin, WMFC	1	2		16ns
6.	MDRout, SelectY, Add, Zin	1	1		2ns
7.	Zout, R1in, End	1	1		2ns
	total Cycles	7	9		

assume

(2)- Memory read, or Write takes the same time as one internal processor (total execution time) = 7 clock cycles * t_i

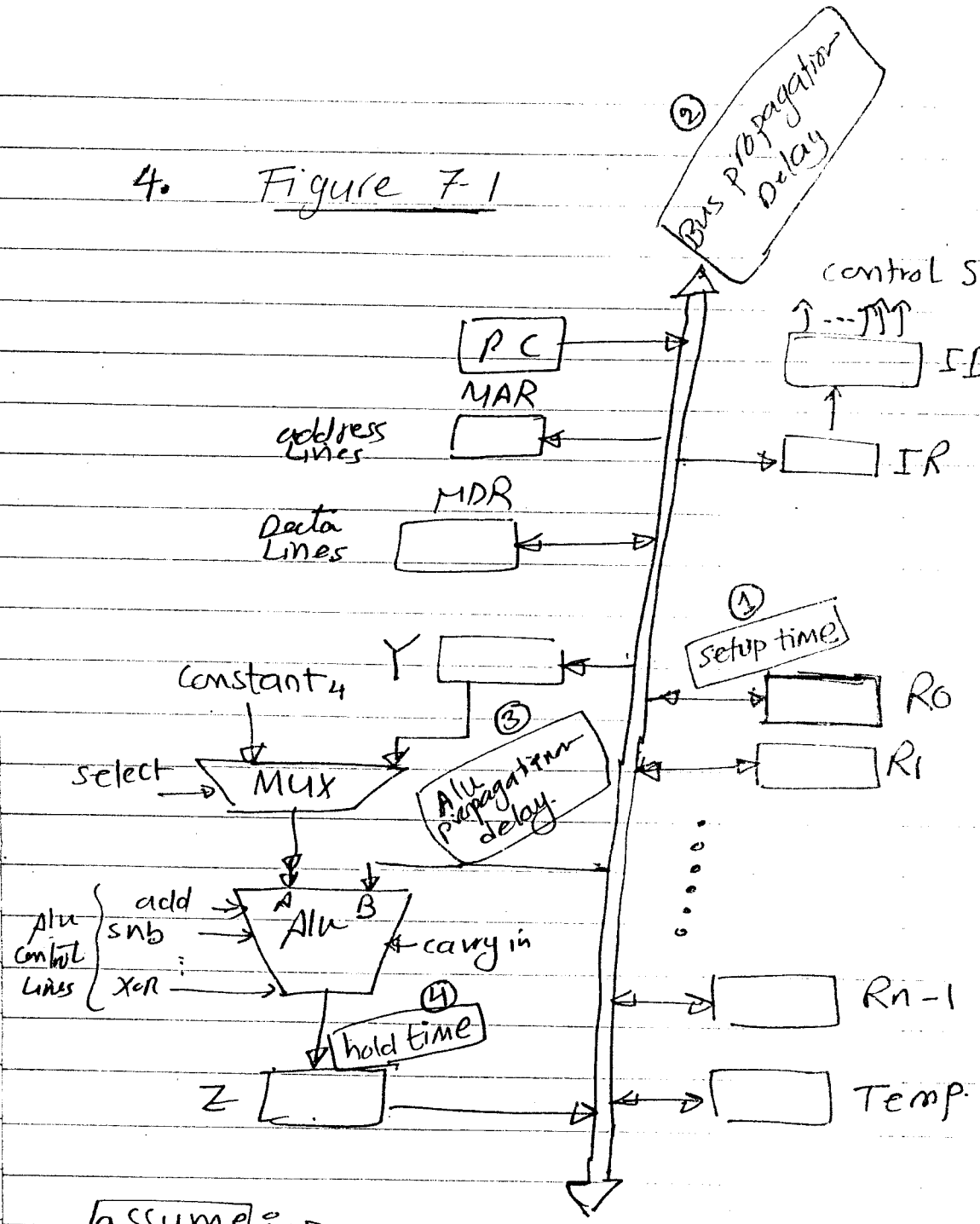
زمن الـ cycle الواحدة

(3.) memory access time = 2 processor clock period.

estimate total execution time = 9 clock cycles * t_i

(7.) the processor wait in step (2) & (5) = 2 * 16 nsec = 32 nsec
other steps = 5 * 2 nsec = 10 nsec
total time = 32 ns + 10 ns = 42 ns

4. Figure 7-1



assume :→

① propagation Delay along the bus = 0.
② propagation Delay through the ALU = 2 nsec
③ setup time for register = 0.1 nsec
④ Hold time is = 0 nsec

Reg

What is the minimum clock period needed for transfering data from one register to the register Z = 0.3 + 2 + 0.2 + c = 2.5 n

5. For Figure 7-1

Write the sequence of control steps required for the bus structure in Figure 7-1

(a) Add #NUM, R_1 (immediate)

Steps	action
1-	PCout, MARin, read select4, Add, Zin
2-	Zout, PCin, Yin, WMFC
3-	MDRout, IRin
4-	Select constant (num), R_1out, Add, Zin
5-	Zout, R_1in, End.

(b) Add NUM, R_1

Steps	action
1-	PCout, MARin, Read, Select4, ADD, Zin
2-	Zout, PCin, Yin, WMFC
3-	MDRout, IRin
4-	offset-field-of IRout, MARin, Read
5-	R_1out, Yin, WMF
6-	MDRout, SelectY,
7-	Zout, R_1in, End.

(c) Add (num), R_1

steps	action
1-	PCout, MARin, Read, Select4, Add, Zin
2-	Zout, PCin, Yin, WMFC
3-	MDRout, IRin
4-	Offset field of IRout, MARin, Read
5-	WMFC.
6-	MDRout, MARin, Read
7-	R1out, Yin, WMFC
8-	MDRout, SelectY, Add, Zin
9-	Zout, R1in, End.

For 3 instructions 5-(a), 5-(b), 5-(c)

6 Suggest a scheme that exploits these common steps to reduce the complexity of the encoder block figure 7-11.

يتم عمل ذلك باعتبار كلاً من (a)، (b)، (c) على أنهم أمر واحد وهو (add) ولكن له 3-addressing modes.

- immediate
- (Abs) Direct
- Indirect

[Suggest]

1. PCout, MARin, Read, Select4, Add, Zin
2. Zout, PCin, Yin, WMFC
3. MDRout, IRin
4. PCout, MARin, Read, Select 4, Add, Zin
5. Zout, PCin, If imm branch to 10

6. WMFC
7. MDRout, MARin, Read, if Abs branch to 10
8. WMFC
9. MDRout, MARin, Read
10. R1out, Yin, WMFC
11. MDRout, Select Y, Add, Zin
12. Zout, R1in, End.

direct

problem (7)

assume
- each control step = 2 nsec
- example figure 7-6
- assume wait in steps (2) and (5) = 16 nsec

steps actions

wait in step (2) & (5) = 2 * 16 nsec = 32 nsec.

exec. time in steps 1, 3, 6, 7 = 5 * 2 nsec = 10 nsec

total time = 32 nsec + 10 = 42 nsec.

processor idle time = $\frac{32}{42}$